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09/712,509	11/14/2000	Danilo Pau	99AG29553247	9109

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CHRISTOPHER F. REGAN
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
P.O. Box 3791
Orlando, FL 32802-3791

EXAMINER	
RAO, ANAND SHASHIKANT	
ART UNIT	**PAPER NUMBER**
2613	7

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/712,509	Applicant(s) PAU ET AL.	
	Examiner Andy S. Rao	Art Unit 2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

Priority

2. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 11-37 have been renumbered 10-36.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadono in view of Adolph et al., (hereinafter referred to as "Adolph").

Kadono discloses a method for producing an output bitstream of a coded digital video data having a bit-rate different from a bit-rate different of an input bitstream of coded digital video data (Kadono: column 6, lines 40-50), the method comprising: dividing the input bitstream into a sequence of coded data and a sequence of control bits (Kadono: column 18, lines 60-65); modifying the sequence of control bits as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits (Kadono: column 17, lines 5-29); decoding the sequence of coded data for producing an intermediate sequence of data (Kadono: column 18, lines 50-60); quantizing with a pre-established step and coding the intermediate sequence of data for producing an output sequence of coded data (Kadono: column 21, lines 40-50), as in claim 10. However, Kadono fails to specifically disclose merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream of the coded digital video data having the desired bit-rate. Adolph discloses merging control information (Adolph: column 2, lines 57-65) with the coded video digital data (Adolph: column 3, lines 1-20) in a similar transcoding method in order efficiently allow for further post processing of the coded

video data (Adolph: column 1, lines 1-65). Accordingly, given this teaching, it would have been obvious to one of ordinary skill in the art to incorporate Adolph's merging operation of control bits into the Kadono method, in order to allow for efficient post processing in Kadono's method. The Kadono method, now incorporating Adolph's merging, has all of the features of claim 10.

Regarding claim 11, the Kadono method, now incorporating Adolph's merging, has the data being dequantized (Kadono: column 18, lines 60-65), as specified.

Regarding claims 12-13, the Kadono method, now incorporating Adolph's merging, has both MPEG and MPEG-2 data (Kadono: column 2, lines 5-20), as in the claims.

Regarding claim 14, the Kadono method, now incorporating Adolph's merging, has Huffman decoding followed by a run-length decoding (Kadono: column 2, lines 65-67; column 3, lines 1-2) and run length coding followed by a Huffman coding (Kadono: column 3, lines 20-27), as in the claim.

Regarding claim 15, the Kadono method, now incorporating Adolph's merging, has a feed back rate control technique (Kadono: column 4, lines 20-39), as in the claim.

Regarding claim 16, the Kadono method, now incorporating Adolph's merging, has a feed-back/forward hybrid rate control technique (Kadono: column 3, lines 35-40;column 4, lines 20-39), as in the claim.

Kadono discloses a method for producing an output bitstream of a coded digital video data having a bit-rate different from a bit-rate different of an input bitstream of coded digital video data (Kadono: column 6, lines 40-50), the method comprising: dividing the input bitstream into a sequence of coded data and a sequence of control bits (Kadono: column 18, lines 60-65); modifying the sequence of control bits as a function of the desired bit-rate of the output bitstream

for producing an output sequence of control bits (Kadono: column 17, lines 5-29); decoding the sequence of coded data for producing an intermediate sequence of data (Kadono: column 18, lines 50-60) using a Huffman decoding followed by a run-length decoding (Kadono: column 2, lines 65-67; column 3, lines 1-2); quantizing with a pre-established step and coding the intermediate sequence of data using a run length coding followed by a Huffman coding (Kadono: column 3, lines 20-27) for producing an output sequence of coded data (Kadono: column 21, lines 40-50), as in claim 17. However, Kadono fails to specifically disclose merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream of the coded digital video data having the desired bit-rate. Adolph discloses merging control information (Adolph: column 2, lines 57-65) with the coded video digital data (Adolph: column 3, lines 1-20) in a similar transcoding method in order efficiently allow for further post processing of the coded video data (Adolph: column 1, lines 1-65). Accordingly, given this teaching, it would have been obvious to one of ordinary skill in the art to incorporate Adolph's merging operation of control bits into the Kadono method, in order to allow for efficient post processing in Kadono's method. The Kadono method, now incorporating Adolph's merging, has all of the features of claim 17

Regarding claim 18, the Kadono method, now incorporating Adolph's merging, has the data being dequantized (Kadono: column 18, lines 60-65), as specified.

Regarding claims 19-20, the Kadono method, now incorporating Adolph's merging, has both MPEG and MPEG-2 data (Kadono: column 2, lines 5-20), as in the claims.

Regarding claim 21, the Kadono method, now incorporating Adolph's merging, has a feed back rate control technique (Kadono: column 4, lines 20-39), as in the claim.

Regarding claim 22, the Kadono method, now incorporating Adolph's merging, has a feed-back/forward hybrid rate control technique (Kadono: column 3, lines 35-40;column 4, lines 20-39), as in the claim.

Kadono discloses a device for producing an output bitstream of a coded digital video data having a bit-rate different from a bit-rate different of an input bitstream of coded digital video data (Kadono: figures 1 and 4), the device comprising: a first circuit for separating the input bitstream into a sequence of coded data and a sequence of control bits (Kadono: column 18, lines 60-65); a second circuit having an input for receiving the sequence of control bits, said second circuit generating a modified sequence of control bits as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits (Kadono: column 17, lines 5-29); a decoder having an input for receiving the sequence of coded data and an output for providing an intermediate sequence of data (Kadono: column 18, lines 50-60); a quantizer for quantizing with a pre-established step and coding the intermediate sequence of data for producing an output sequence of coded data (Kadono: column 21, lines 40-50), as in claim 23. However, Kadono fails to specifically disclose a third circuit merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream of the coded digital video data having the desired bit-rate. Adolph discloses a third circuit for merging control information (Adolph: column 2, lines 57-65) with the coded video digital data (Adolph: column 3, lines 1-20) in a similar transcoder in order efficiently allow for further post processing of the coded video data (Adolph: column 1, lines 1-65). Accordingly, given this teaching, it would have been obvious to one of ordinary skill in the art to incorporate Adolph's third circuit for merging control bits into the Kadono device, in order to allow for efficient post processing in

Kadono's device. The Kadono device, now incorporating Adolph's a third circuit for merging, has all of the features of claim 23.

Regarding claim 24, the Kadono device, now incorporating Adolph's a third circuit for merging, has a dequantizer for the dequantizing the data (Kadono: column 18, lines 60-65), as specified.

Regarding claims 25-26, the Kadono device, now incorporating Adolph's a third circuit for merging, has input and output bitstreams being both MPEG and MPEG-2 data (Kadono: column 2, lines 5-20), as in the claims.

Regarding claims 27-28, the Kadono device, now incorporating Adolph's a third circuit for merging, has Huffman decoder followed by a run-length decoder (Kadono: column 2, lines 65-67; column 3, lines 1-2) and run length coder followed by a Huffman coder (Kadono: column 3, lines 20-27), as in the claims.

Regarding claim 29, the Kadono device, now incorporating Adolph's a third circuit for merging, has a bit rate control circuit connected to the encoder (Kadono: column 4, lines 20-39), as in the claim.

Regarding claim 30, the Kadono device, now incorporating Adolph's a third circuit for merging, has a multiplexer as in the claim (Adolph: column 2, lines 50-55), as in the claim.

Kadono discloses a device for producing an output bitstream of a coded digital video data having a bit-rate different from a bit-rate different of an input bitstream of coded digital video data (Kadono: figures 1 and 4), the device comprising: a first circuit for separating the input bitstream into a sequence of coded data and a sequence of control bits (Kadono: column 18, lines 60-65); a second circuit having an input for receiving the sequence of control bits, said second

circuit generating a modified sequence of control bits as a function of the desired bit-rate of the output bitstream for producing an output sequence of control bits (Kadono: column 17, lines 5-29); a decoder having an input for receiving the sequence of coded data and an output for providing an intermediate sequence of data (Kadono: column 18, lines 50-60) said decoder comprising a Huffman decoder and a run-length decoder connected in series thereto (Kadono: column 2, lines 65-67; column 3, lines 1-2); a quantizer for quantizing with a pre-established step; and encoder connected to the output of said quantizer for coding the intermediate sequence of data for producing an output sequence of coded data (Kadono: column 21, lines 40-50), said encoder comprising a run length coder and a Huffman coder connected in series thereto (Kadono: column 3, lines 20-27),, as in claim 31. However, Kadono fails to specifically disclose a third circuit merging the output sequence of control bits and the output sequence of coded data for producing the output bitstream of the coded digital video data having the desired bit-rate. Adolph discloses a third circuit for merging control information (Adolph: column 2, lines 57-65) with the coded video digital data (Adolph: column 3, lines 1-20) in a similar transcoder in order efficiently allow for further post processing of the coded video data (Adolph: column 1, lines 1-65). Accordingly, given this teaching, it would have been obvious to one of ordinary skill in the art to incorporate Adolph's third circuit for merging control bits into the Kadono device, in order to allow for efficient post processing in Kadono's device. The Kadono device, now incorporating Adolph's a third circuit for merging, has all of the features of claim 31.

Regarding claim 32, the Kadono device, now incorporating Adolph's a third circuit for merging, has a dequantizer for the dequantizing the data (Kadono: column 18, lines 60-65), as specified.

Regarding claims 33-34, the Kadono device, now incorporating Adolph's a third circuit for merging, has input and output bitstreams being both MPEG and MPEG-2 data (Kadono: column 2, lines 5-20), as in the claims.

Regarding claim 35, the Kadono device, now incorporating Adolph's a third circuit for merging, has a bit rate control circuit connected to the encoder (Kadono: column 4, lines 20-39), as in the claim.

Regarding claim 37, the Kadono device, now incorporating Adolph's a third circuit for merging, has a multiplexer as in the claim (Adolph: column 2, lines 50-55), as in the claim.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Takahashi discloses an image conversion apparatus for transforming compressed image data of different resolutions. Hanamura discloses an apparatus and method for transcoding.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy S. Rao whose telephone number is (703)-305-4813. The examiner can normally be reached on Monday-Friday 8 hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris S. Kelley can be reached on (703)-305-4856. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-4700.

Andy S. Rao
Primary Examiner
Art Unit 2613

ANDY RAO
PRIMARY EXAMINER

asr
September 24, 2003